WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a ferroelectric element, an electric field applied to the ferroelectric element being controlled to relatively shift a position of a first atom with respect to a position of another atom and to store data at stabilized positions as remanent polarization,

wherein the ferroelectric element stores two-bit information by having total four stabilized positions of the first atom, which include first stabilized two positions in a first direction and second stabilized two positions in a second direction perpendicular to the first direction.

2. A semiconductor memory device comprising:

a ferroelectric element composed of a ferroelectric material having one structure selected from an ABO_3 crystal structure and an ABO_3 perovskite structure, both of the ABO_3 crystal structure and the ABO_3 perovskite structure being composed of atoms A, atoms B and atoms O, an electric field applied to the ferroelectric element being controlled so that a position of each of the atoms B is relatively shifted for positions of the atoms A and the atoms O to store data at the stabilized positions as remanent polarization,

wherein the ferroelectric element stores two-bit information by having total four stabilized positions

of the atoms B, which include first stabilized two positions in a first direction and second stabilized two positions in a second direction perpendicular to the first direction.

3. A semiconductor memory device comprising:

a ferroelectric element composed of a ferroelectric material having one structure selected from an $ABxC(1-x)O_3$ crystal structure and an $ABxC(1-x)O_3$ perovskite structure, both of the $ABxC(1-x)O_3$ crystal structure and the $ABxC(1-x)O_3$ perovskite structure being composed of at least atoms A, atoms B, atoms C and atoms O, an electric field applied to the ferroelectric element being controlled to relatively shift a position of one atom selected from the atoms B and atoms C with respect to positions of the atoms A and atoms O and permit data to be stored in stabilized positions as remanent polarization,

wherein the ferroelectric element stores two-bit information by having total four stabilized positions of one atom selected from the atoms B and atoms C, which include first stabilized two positions in a first direction and second stabilized two positions in a second direction perpendicular to the first direction.

4. The semiconductor memory device according to claim 1, wherein the operation of shifting the first atom to the four positions is performed by use of a first electric field, a second electric field in

a direction opposite to the first electric field, a third electric field in a direction perpendicular to the first electric field, and a fourth electric field in a direction opposite to the third electric field.

5. The semiconductor memory device according to claim 2, wherein the operation of shifting the atom B to the four positions is performed by use of a first electric field, a second electric field in a direction opposite to the first electric field, a third electric field in a direction perpendicular to the first electric field, and a fourth electric field in a direction opposite to the third electric field.

6. The semiconductor memory device according to claim 3, wherein the operation of shifting the selected one atom to the four positions is performed by use of a first electric field, a second electric field in a direction opposite to the first electric field, a third electric field in a direction perpendicular to the first electric field, and a fourth electric field in a direction opposite to the third electric field.

7. The semiconductor memory device according to claim 1, wherein the operation of shifting the first atom to the four positions is performed by use of electric fields generated by controlling voltages applied to four electrodes arranged near the ferroelectric element.

8. The semiconductor memory device according to

claim 2, wherein the operation of shifting the atom B to the four positions is performed by use of electric fields generated by controlling voltages applied to four electrodes arranged near the ferroelectric element.

9. The semiconductor memory device according to claim 3, wherein the operation of shifting the selected one atom to the four positions is performed by use of electric fields generated by controlling voltages applied to four electrodes arranged near the ferroelectric element.

10. The semiconductor memory device according to claim 1, wherein the ferroelectric element includes at least $BaTiO_3$.

11. The semiconductor memory device according to claim 2, wherein the ferroelectric element includes at least $BaTiO_3$.

12. The semiconductor memory device according to claim 3, wherein the ferroelectric element includes at least $BaTiO_3$.

13. The semiconductor memory device according to claim 1, wherein the ferroelectric element includes at least $PbZrxTi(1-x)O_3$.

14. The semiconductor memory device according to claim 2, wherein the ferroelectric element includes at least $PbZrxTi(1-x)O_3$.

15. The semiconductor memory device according to

claim 1, wherein the ferroelectric element includes at least $(BiLa)_4Ti_3O_{12}$, $Bi_4Ti_3O_{12}$, $SrBi_2Ta_2O_9$.

16. A semiconductor memory device comprising:

a ferroelectric element having one structure selected from an ABO_3 crystal structure and an ABO_3 perovskite structure, both of the ABO_3 crystal structure and the ABO_3 perovskite structure being composed of at least atoms A, atoms B and atoms O, an electric field applied to the ferroelectric element being controlled to relatively shift a position of the atoms B with respect to positions of the atoms A and atoms O and permit data to be stored in stabilized positions as remanent polarization,

wherein the ferroelectric element stores multi-bit information by having total six stabilized positions of the atoms B, which include first stabilized two positions in a first direction, second stabilized two positions in a second direction perpendicular to the first direction and third stabilized two positions in a third direction perpendicular to the first and second directions.

17. A semiconductor memory device comprising:

a ferroelectric element having one structure selected from an $ABxC(1-x)O_3$ crystal structure and an $ABxC(1-x)O_3$ perovskite structure, both of the $ABxC(1-x)O_3$ crystal structure and the $ABxC(1-x)O_3$ perovskite structure being composed of at least atoms

A, atoms B, atoms C and atoms O, an electric field applied to the ferroelectric element being controlled to relatively shift a position of one atom selected from the atoms B and atoms C with respect to positions of the atoms A and atoms O and permit data to be stored in stabilized positions as remanent polarization,

wherein the ferroelectric element stores multi-bit information by having total six stabilized positions of one atom selected from the atoms B and atoms C, which include two stabilized positions in a first direction, two stabilized positions in a second direction perpendicular to the first direction and two stabilized positions in a third direction perpendicular to the first and second directions.

18. A semiconductor memory device comprising:

a ferroelectric element, an electric field applied to the ferroelectric element being controlled to relatively shift a position of a first atom with respect to a position of another atom and permit data to be stored in stabilized positions as remanent polarization,

wherein the ferroelectric element stores multi-bit information by having total six stabilized positions of the first atom, which include first stabilized two positions in a first direction, second stabilized two positions in a second direction perpendicular to the first direction and third stabilized two positions in

a third direction perpendicular to the first and second directions.

19. The semiconductor memory device according to claim 16, wherein the operation of shifting the atom to the six positions is performed by use of a first electric field, a second electric field in a direction opposite to the first electric field, a third electric field in a direction perpendicular to the first electric field, a fourth electric field in a direction opposite to the third electric field, a fifth electric field in a direction perpendicular to the first and third electric fields, and a sixth electric field in a direction opposite to the fifth electric field.

20. The semiconductor memory device according to claim 17, wherein the operation of shifting the atom to the six positions is performed by use of a first electric field, a second electric field in a direction opposite to the first electric field, a third electric field in a direction perpendicular to the first electric field, a fourth electric field in a direction opposite to the third electric field, a fifth electric field in a direction perpendicular to the first and third electric fields, and a sixth electric field in a direction opposite to the fifth electric field.

21. The semiconductor memory device according to claim 18, wherein the operation of shifting the atom to the six positions is performed by use of a first

electric field, a second electric field in a direction opposite to the first electric field, a third electric field in a direction perpendicular to the first electric field, a fourth electric field in a direction opposite to the third electric field, a fifth electric field in a direction perpendicular to the first and third electric fields, and a sixth electric field in a direction opposite to the fifth electric field.

22. The semiconductor memory device according to claim 16, wherein the operation of shifting the atom to the six positions is performed by use of electric fields generated by controlling voltages applied to six electrodes arranged near the ferroelectric element.

23. The semiconductor memory device according to claim 17, wherein the operation of shifting the atom to the six positions is performed by use of electric fields generated by controlling voltages applied to six electrodes arranged near the ferroelectric element.

24. The semiconductor memory device according to claim 18, wherein the operation of shifting the atom to the six positions is performed by use of electric fields generated by controlling voltages applied to six electrodes arranged near the ferroelectric element.

25. The semiconductor memory device according to claim 16, wherein the ferroelectric element includes at least $BaTiO_3$.

26. The semiconductor memory device according to

claim 17, wherein the ferroelectric element includes at least $BaTiO_3$.

27. The semiconductor memory device according to claim 18, wherein the ferroelectric element includes at least $BaTiO_3$.

28. The semiconductor memory device according to claim 17, wherein the ferroelectric element includes at least $PbZrxTi(1-x)O_3$.

29. The semiconductor memory device according to claim 18, wherein the ferroelectric element includes at least $PbZrxTi(1-x)O_3$.

30. The semiconductor memory device according to claim 18, wherein the ferroelectric element includes at least $(BiLa)_4Ti_3O_{12}$, $Bi_4Ti_3O_{12}$, $SrBi_2Ta_2O_9$.

31. A semiconductor memory device which stores information of at least three values, comprising:

a ferroelectric element, and

at least three electrodes in contact with the ferroelectric element.

32. A semiconductor memory device comprising:

a ferroelectric element, and

at least three electrodes in contact with the ferroelectric element,

wherein at least one of the electrodes is connected to a data readout line via a transistor.

33. A semiconductor memory device comprising:

a ferroelectric element,

wherein a first atom is shifted to at least three positions on a two-dimensional plane in the ferroelectric element to hold data of at least three values.

34. A semiconductor memory device comprising:

a ferroelectric element,

wherein a first atom is shifted to at least three positions on a three-dimensional plane in the ferroelectric element to hold data of at least three values.

35. A semiconductor memory device comprising:

a ferroelectric element, and

first, second, third and fourth electrodes,

wherein the first and second electrodes are respectively connected to source and drain terminals of a first transistor and the third and fourth electrodes are respectively connected to source and drain terminals of a second transistor to configure one memory cell and information of at least two bits is stored in the memory cell.

36. The semiconductor memory device according to claim 35, wherein a plurality of memory cells which each have the same configuration as the above memory cell are provided, the source and drain terminals of the first transistor are used as a first two-terminal, the source and drain terminals of the second transistor are used as a second two-terminal, a first two-terminal of a plurality of memory cells are series-connected to one another and a second two-terminal of the memory

cells are series-connected to one another to provide a memory cell unit.